

ATME COLLEGE OF ENGINEERING

13th KM Stone, Bannur Road, Mysore - 570 028



A T M E
College of Engineering

**DEPARTMENT OF ELECTRICAL & ELECTRONICS
ENGINEERING**

NOTES

COURSE: Analog Electronic Circuits

COURSE CODE: 1BEE302

SEMESTER: III

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

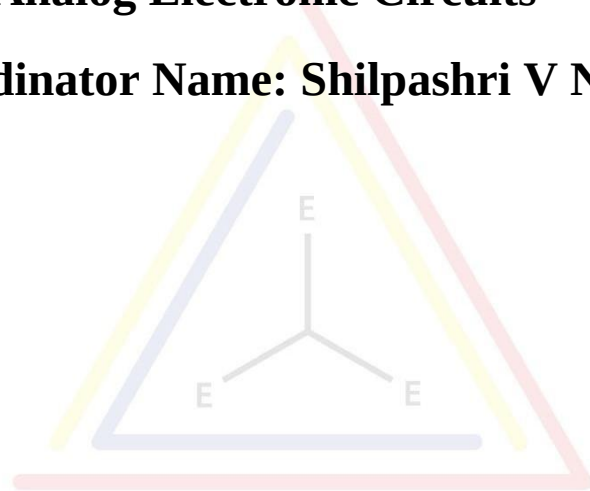
NOTES

Academic Year: 2026-27

Course Code: 1BEE302

Course Title: Analog Electronic Circuits

Course Co-ordinator Name: Shilpashri V N



Department of EEE
Emitting Elite Energy

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Vision of the Institute Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources. Mission of the Institute • To keep pace with advancements in knowledge and make the students competitive and capable at the global level. • To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torch-bearers of tomorrow's society. • To strive to attain ever-higher benchmarks of educational excellence	Vision of the Department To create Electrical and Electronics Engineers who excel to be technically competent and fulfil the cultural and social aspirations of the society. Mission of the Department • To provide knowledge to students that builds a strong foundation in the basic principles of electrical engineering, problem solving abilities, analytical skills, soft skills and communication skills for their overall development. • To offer outcome based technical education. • To encourage faculty in training & development and to offer consultancy through research & industry interaction.
Program Educational Objectives (PEO's) • PEO1: To produce competent and ethical Electrical and Electronics Engineers who will exhibit the necessary technical and managerial skills to perform their duties in society. • PEO2: To make graduates continuously acquire and enhance their technical and socio-economic skills. • PEO3: To aspire graduates on R&D activities leading to offering solutions and excel in various career paths. • PEO4: To produce quality engineers who have the capability to work in teams and contribute to real time projects.	Program Specific Outcomes (PSO's) • PSO1: Apply the concepts of Electrical & Electronics Engineering to evaluate the performance of power systems and also to control industrial drives using power electronics. • PSO2: Demonstrate the concepts of process control for Industrial Automation, design models for environmental and social concerns and also exhibit continuous self- learning.

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Program Outcomes (PO's)

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

Module-2

BJT Biasing: Introduction to biasing, operating point, bias configurations; fixed-bias, emitter bias, voltage divider bias, DC bias with voltage feedback, design of bias circuits, effect of temperature on bias; thermal runaway, bias stabilization, stability, stability factors of bias circuits.

BJT AC Analysis: Amplification in AC domain, Transistor modelling for small signal analysis; resistance, model of CB, CE, and CC configurations, hybrid equivalent model CB, CE, and CC configurations, hybrid π model. Low frequency analysis, high frequency analysis.

Transistor Biasing and Stabilization

The biasing of a bipolar junction transistor is to establish the desired value of **collector to emitter voltage V_{CE} and Collector current I_C** , to ensure that the amplifier will have proper gain and input impedance with undistorted output voltage swing. **The values of V_{CE} and I_C together are known as operating point or quiescent point (Q-point).** The operating point must be stable for proper operation of the transistor. However, the operating point shifts with changes in transistor parameters such as β (Current Gain), I_{CO} & V_{BE} .

Operating Point

The transistor can be operated in three regions cut-off, active and saturation regions. In order to operate transistor in the desired region we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor. Let us consider the common emitter configuration of NPN transistor and its output characteristics as shown in Fig.1.

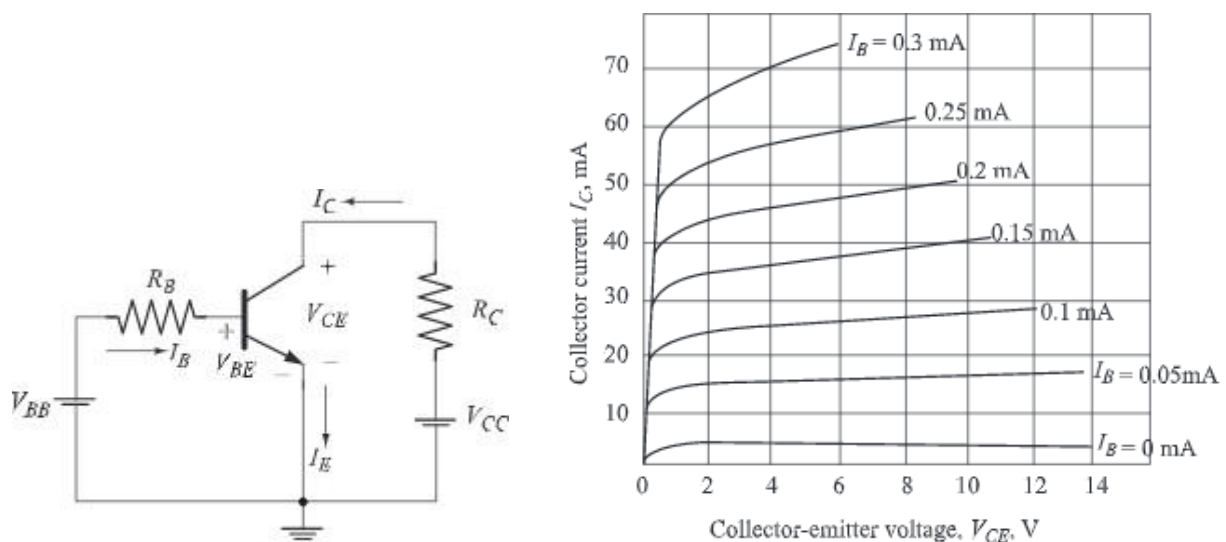


Fig.1: Common-Emitter configuration and its output characteristics.

The region in the characteristics above $I_B = 0$ mA and to the right of the few tenths of volts of V_{CE} is the active region. In this region the collector current increases with increase in the base current. The base-emitter junction is forward biased and base-collector junction is reverse biased in this region.

The region where the base-emitter junction is reverse biased below 0.1V for germanium and below 0V for silicon is the cut-off region. In this region base-emitter junction and base-collector junction is reverse biased. The emitter current is zero and the transistor is non-conducting in this region.

The region very close to $V_{CE} = 0$ where all curves appear to merge and fall rapidly to the origin is called saturation region. In this region base-emitter and base-collector junctions are forward biased. The collector current is considerably large and V_{CE} is few tenths of volts.

The transistor is required to be biased from cut-off to saturation and vice-versa when it is being used as a switch. It must be biased in the active region when it is being used as an amplifier. The transistor functions linearly when its operation is restricted to the active region.

There are several circuit configurations through which the transistor current and voltage can be adjusted in order to fix the operating point. Fixed bias, emitter bias or self-bias and voltage divider bias are some configurations.

Fixed Bias Configuration:

The fixed bias circuit is shown in Fig.2(a). It is the simplest dc bias configuration. For the dc analysis we can replace capacitor with an open circuit (since capacitor blocks dc) because the reactance of capacitor is infinity. The dc equivalent circuit is shown in Fig.2(b).

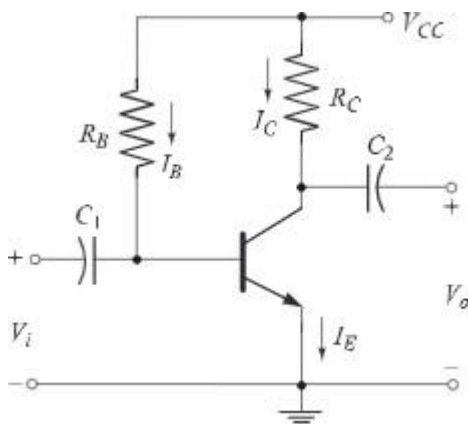


Fig.2(a): Fixed bias circuit

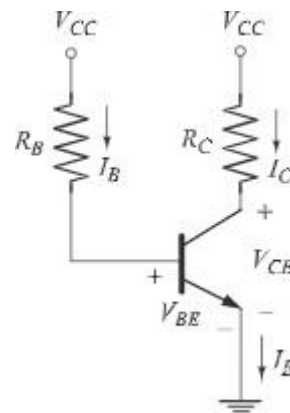


Fig.2(b): DC equivalent circuit of fixed bias

Apply KVL to the base circuit we get;

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The magnitudes of collector current and base current neglecting I_{CO} are related by,

$$I_C = \beta I_B$$

Where, β = dc current gain of Common Emitter configuration. I_B is decided by R_B and I_C is decided by β . Thus R_C has no role in the value of I_C when the transistor is in active region.

Applying KVL to the circuit shown in Fig.2 (a) we get;

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

The transistor circuit operating in saturation region is shown in Fig.2 (c). Apply KVL to the circuit we get;

$$V_{CC} - I_{C(sat)} R_C - V_{CE(sat)} = 0$$

$$I_{(sat)} = \frac{V_{CC} - V_{(sat)}}{R_C}$$

$$\text{But } V_{CE(sat)} \approx 0$$

$$I_{C(sat)} \approx \frac{V_{CC}}{R_C}$$

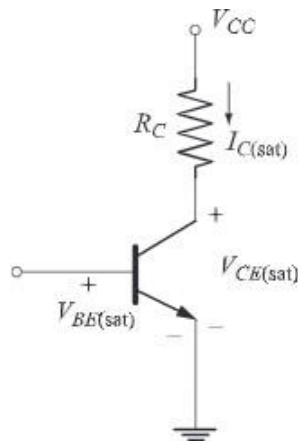
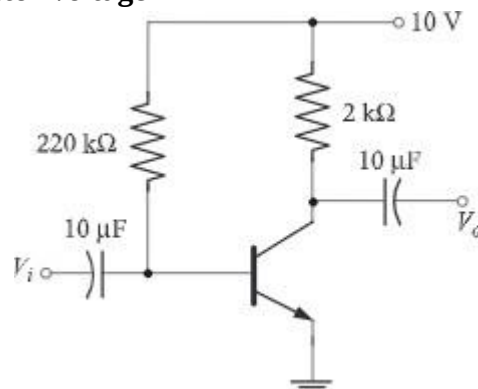


Fig.2 (c): Transistor operating in Saturation region.

Solved Examples:

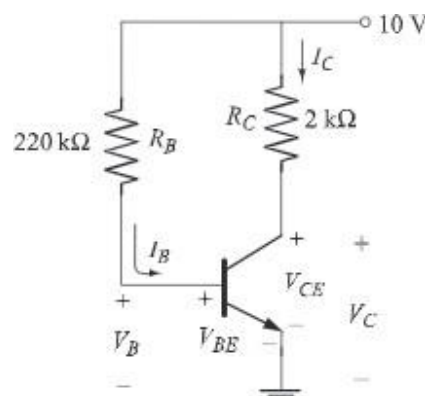
1. For the fixed bias circuit shown, assuming $V_{BE} = 0.7V$ and $\beta = 60$ find:

- Quiescent values of base and collector currents.
- Quiescent value of V_{CE} .
- Base-ground and collector-ground voltages.
- Base-collector voltage



- Quiescent values of I_C and V_{CE} for $\beta = 110$.

Solution: Consider the coupling capacitors as open circuit and mention various currents and voltages in the circuit as shown below.



a. Quiescent values of base current and collector current.

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega} = 42.27\text{ }\mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 60 \times 42.27\text{ }\mu\text{A} = 2.54\text{ mA}$$

b. Quiescent value of V_{CE} .

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10 - (2.54\text{ mA})(2\text{ k}\Omega) = 4.92\text{ V}$$

c. Base and collector voltages with respect to ground.

$$V_B = V_{BE} = 0.7\text{ V}$$

$$V_C = V_{CE} = 4.92\text{ V}$$

d. Base-collector voltage.

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 4.92\text{ V} = -4.22\text{ V}$$

e. When $\beta = 110$.

I_{BQ} is not affected by change in β .

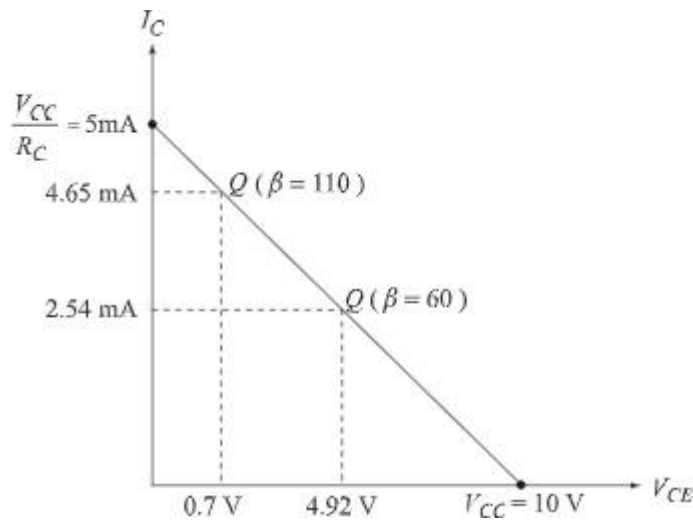
$$I_{BQ} = 42.27\text{ }\mu\text{A} \quad [\text{as obtained in part (a)}]$$

$$I_{CQ} = \beta I_{BQ} = 110 \times 42.27\text{ }\mu\text{A} = 4.65\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (4.65\text{ mA} \times 2\text{ k}\Omega) = 0.7\text{ V}$$

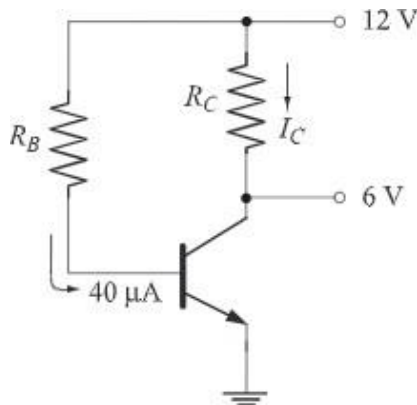
β	I_{BQ}	I_{CQ}	V_{CEQ}
60	42.27 μA	2.54 mA	4.92 V
110	42.27 μA	4.65 mA	0.7 V

The Q-points are indicated in the dc load line as shown in the figure.



Observe that when β changes from 60 to 110, the Q-point shifts from the middle of the active region to near saturation region. Therefore the fixed bias circuit has very poor stability of operating point.

2. For the fixed bias circuit shown, find collector current, collector resistance, base resistance and V_{CE} . Assume $\beta = 80$ and $V_{BE} = 0.7 \text{ V}$



Solution:

Collector current:

$$I_C = \beta I_B = (80)(40 \mu\text{A}) = 3.2 \text{ mA}$$

Collector resistance:

$$\begin{aligned} V_C &= 6 \text{ V} \\ V_{CE} &= V_C = 6 \text{ V} \\ R_C &= \frac{V_{CC} - V_{CE}}{I_C} = \frac{12 \text{ V} - 6 \text{ V}}{3.2 \text{ mA}} = 1.875 \text{ k}\Omega \end{aligned}$$

Base Resistance:

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12\text{ V} - 0.7\text{ V}}{40\text{ }\mu\text{A}} = 282.5\text{ k}\Omega$$

$$\begin{aligned} V_{CE} &= \text{Voltage from collector to emitter} \\ &= V_C = 6\text{ V.} \end{aligned}$$

Emitter Stabilized Bias Configuration

To improve the stability of the biasing circuit over a fixed bias circuit, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as **emitter bias circuit**. The circuit of emitter bias configuration is shown in Fig.3(a).

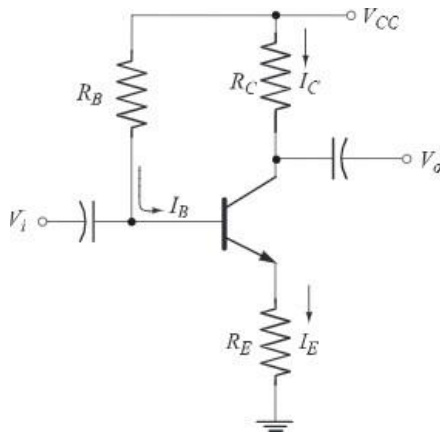


Fig.3 (a): Emitter Bias Circuit.

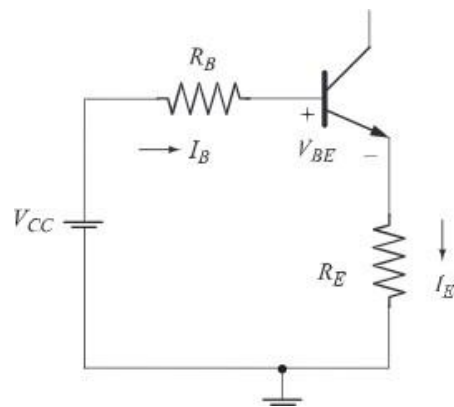


Fig.3 (b): Base-Emitter Circuit.

Circuit Analysis: The base emitter circuit is shown in Fig.3 (b). Applying KVL to the base-emitter circuit we get;

$$\begin{aligned} V_{CC} &= I_B R_B + V_{BE} + I_E R_E \\ I_E &= I_C + I_B \end{aligned}$$

Using $I_C = \beta I_B$;

$$\begin{aligned} I_E &= \beta I_B + I_B \\ I_E &= (\beta + 1) I_B \end{aligned}$$

$$\begin{aligned} V_{CC} &= I_B R_B + V_{BE} + (\beta + 1) I_B R_E \\ V_{CC} - V_{BE} &= I_B [R_B + (\beta + 1) R_E] \\ I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \end{aligned}$$

The collector-emitter circuit is shown in Fig.3 (c).

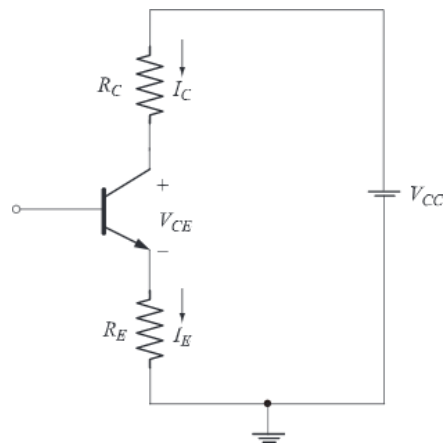


Fig.3(c): Collector-Emitter Circuit

Applying KVL to the collector-emitter circuit we get;

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Substituting $I_E = I_C$.

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Let,

V_C = Voltage from collector to ground

V_B = Voltage from base to ground

V_E = Voltage from emitter to ground

Therefore, V_E = Voltage across R_E

$$V_E = I_E R_E$$

$$\begin{aligned} V_C &= V_{CE} + V_E \\ &= V_{CE} + I_E R_E \end{aligned}$$

Substitute for $(V_{CE} + I_E R_E)$ we get;

$$V_B = V_{CC} - I_B R_B$$

Saturation Level: When transistor is in saturation

$$V_{CE} = V_{CE(sat)} \approx 0 \text{ V}$$

$$I_C = I_{C(sat)}$$

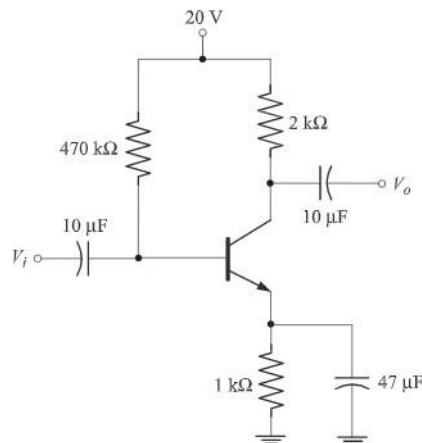
Taking $I_E = I_C$ we have;

$$V_{CC} = I_{C(sat)} [R_C + R_E]$$

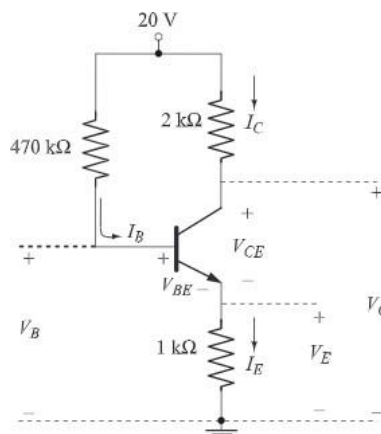
$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}$$

Solved Examples:

1. For the emitter-bias shown using silicon transistor with $V_{BE} = 0.7 \text{ V}$ and $\beta = 60$, find;
 - a. Base current and collector current
 - b. Collector-Emitter voltage
 - c. Collector, emitter and base voltages to ground
 - d. Base-collector voltage



Solution: For dc analysis the capacitors are acts as open circuit.



a. Base current and collector current

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)} = \frac{20 - 0.7}{470k + (1 + 60)1k} = 36.34 \mu A$$

$$I_C = \beta I_B = 60 * 36.34 \mu = 2.18 \text{ mA}$$

b. Collector-emitter voltage

$$\begin{aligned} V_{CE} &= V_{CC} - I_C (R_C + R_E) \\ &= 20 \text{ V} - 2.18 \text{ mA} [2 \text{ k}\Omega + 1 \text{ k}\Omega] \\ &= 13.46 \text{ V} \end{aligned}$$

c. Collector, emitter and base voltages to ground

$$V_C = V_{CC} - I_C R_C = 20 \text{ V} - (2.18 \text{ mA} \times 2 \text{ k}\Omega) = 15.64 \text{ V}$$

$$V_E = V_C - V_{CE} = 15.64 \text{ V} - 13.46 \text{ V} = 2.18 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2.18 \text{ V} = 2.88 \text{ V}$$

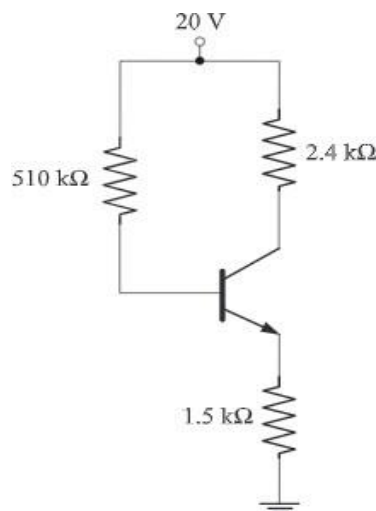
d. Base-collector voltage

$$V_{BC} = V_B - V_C$$

$$V_{BC} = 2.88 - 15.64 = -12.76 \text{ V}$$

2. For the emitter bias circuit shown using silicon transistor $V_{BE} = 0.7 \text{ V}$ and $\beta = 100$. Find;

- Quiescent values of base current, collector current and collector to emitter voltage.
- Voltage at collector, base and emitter with respect to ground.



Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_E} = \frac{20 - 0.7}{510k + (1 + 100)1.5k} = 29.18 \mu A$$

$$I_C = \beta I_B = 100 * 29.18 \mu = 2.92 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 2.92 \text{ m} (2.4k + 1.5k) = 8.61 \text{ V}$$

$$V_E = I_E R_E = [I_B + I_C] R_E = [29.18 \mu + 2.92 \text{ m}] 1.5k = 4.42 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 + 4.42 = 5.12 \text{ V}$$

Voltage Divider Bias Configuration

In the fixed bias and the emitter bias circuits, the collector current and collector-emitter voltage that is operating point is a function of **dc current gain β** of the transistor. The current gain is sensitive to **temperature and its value keeps varying**. A biasing circuit independent or less dependent on β such as the **voltage divider bias circuit** is desirable. The voltage divider circuit is shown in Fig.4 (a).

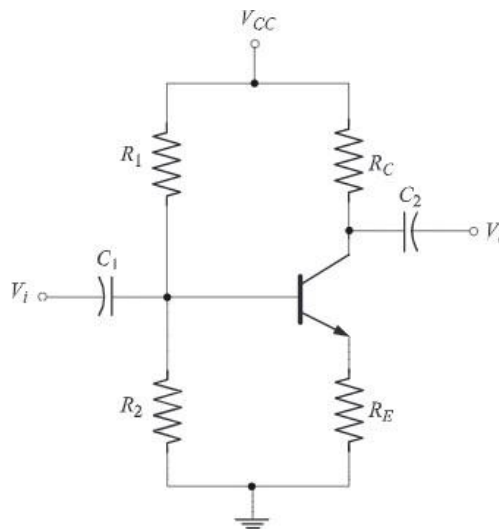


Fig.4 (a): Voltage divider bias circuit

Exact Analysis: The base circuit is redrawn as shown in Fig.4 (b) for the dc analysis. The Thevenin equivalent circuit is shown in Fig.5 (a).

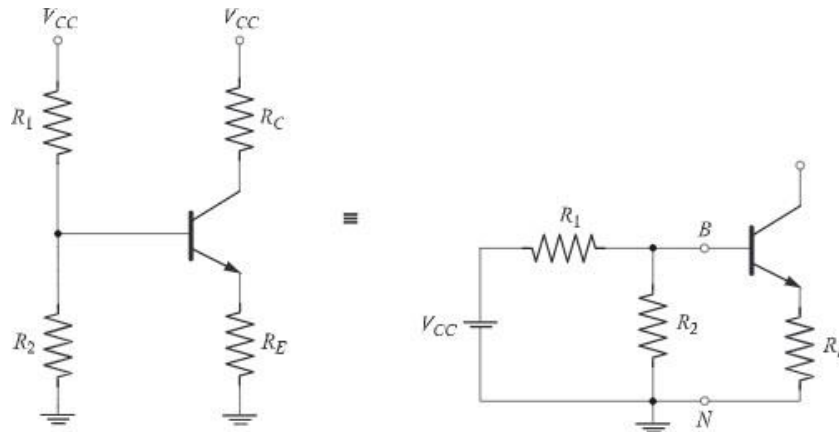


Fig.4 (b): Base circuit of Voltage divider bias configuration

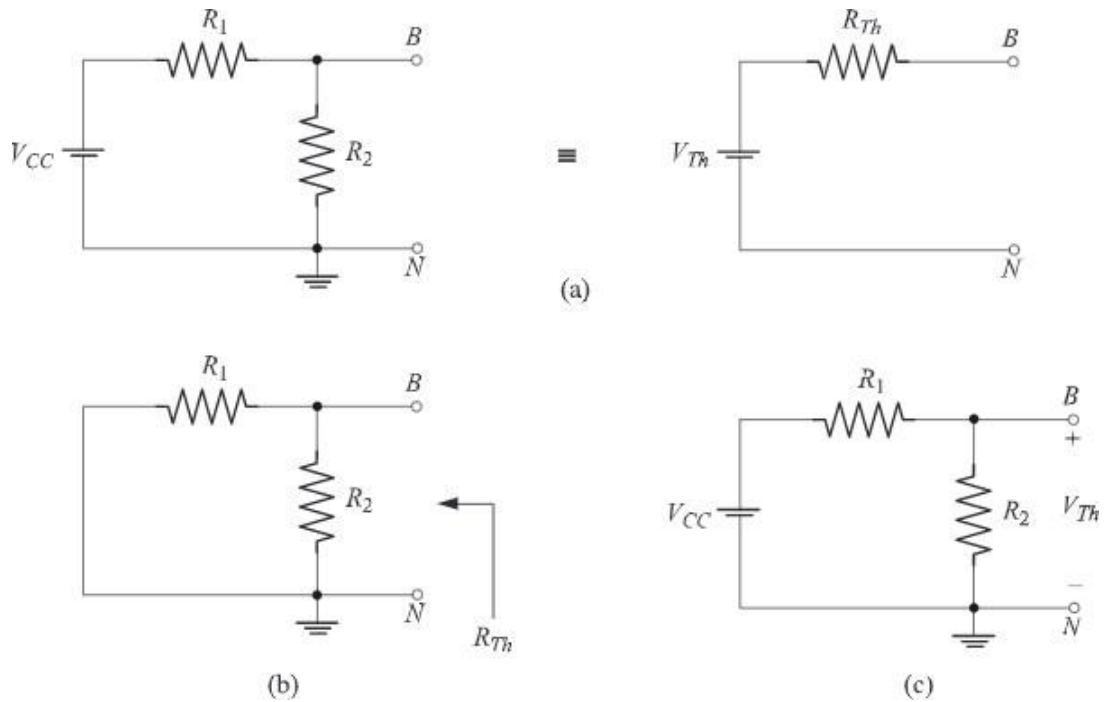


Fig.5: a. Thevenin Equivalent b. Determination of R_{Th} c. Determination of V_{Th}

To find Thevenin resistance R_{Th} , V_{CC} is reduced to zero in the circuit of Fig.5 (a). The resulting circuit is shown in Fig.5 (b).

$$R_{Th} = R_1 \parallel R_2$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

From the Fig.5 (c), the Thevenin Voltage can be obtained,

$$V_{Th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

The circuit shown in Fig.4 (b) can be redrawn as shown in Fig.6 after substituting the Thevenin equivalent between B and N.

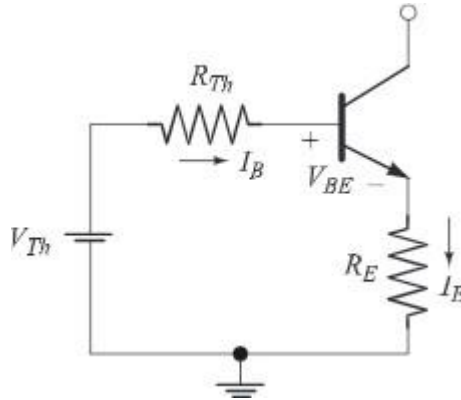


Fig.6: Base circuit with Thevenin Equivalent

Apply KVL to the base circuit shown in Fig.6 we get;

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

$$\text{Now, } I_E = I_C + I_B$$

$$I_C = \beta I_B$$

Substituting in equation 29 we get

$$I_E = \beta I_B + I_B = (1 + \beta) I_B$$

$$V_{Th} = I_B R_{Th} + V_{BE} + (1 + \beta) I_B R_E$$

$$V_{Th} - V_{BE} = I_B [R_{Th} + (1 + \beta) R_E]$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E}$$

The collector circuit is shown in Fig.7. Apply KVL to the circuit we get;

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$I_E = I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Voltage across emitter:

$$V_E = I_E R_E$$

Collector to ground Voltage:

$$V_C = V_{CE} + I_E R_E = V_{CE} + V_E$$

Base to ground Voltage:

$$V_B = V_{BE} + V_E$$

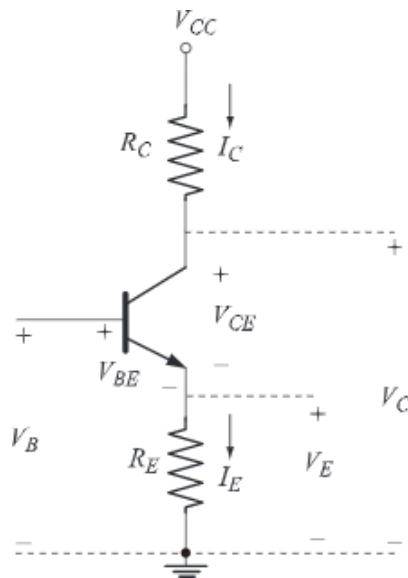


Fig.7: Collector circuit of Voltage Divider Bias Configuration

Transistor Saturation: When transistor is in saturation, $V_{CE} = V_{CE(sat)} \approx 0$ and $I_C = I_{C(sat)}$.

$$V_{CC} = I_{C(sat)}[R_C + R_E]$$

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}$$

Approximate Analysis:

The resistance R_E in the emitter circuit gets reflected as $(1+\beta)R_E$ in the base circuit. Therefore the circuit between base and ground of Fig.4 (b) can be replaced by an equivalent resistance $R_i = (1+\beta)R_E$ as shown in Fig.8.

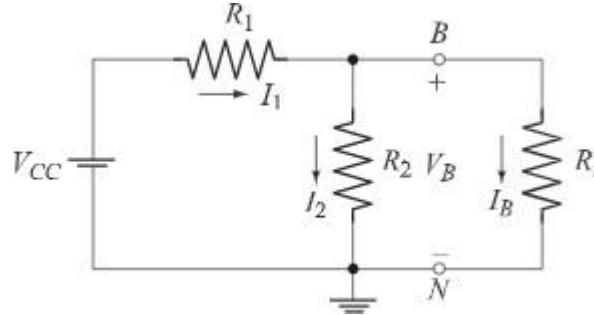


Fig.8: Input circuit of Approximate Analysis

Apply KCL to the above circuit we get;

$$I_1 = I_2 + I_B$$

$$R_i = (1+\beta) R_E \approx \beta R_E, \text{ since } \beta \gg 1$$

$$I_B = \frac{V_B}{R_i} \text{ and } I_2 = \frac{V_B}{R_2}$$

$$\text{If } R_i = (1+\beta) R_E \gg 10 R_2,$$

Then $I_B \ll 0.1 * I_2$, We neglect I_B , as a result we get;

$$I_1 \approx I_2$$

Apply KVL to the above circuit we get;

$$V_{CC} = I_1 R_1 + I_2 R_2$$

$$V_{CC} = I_2 (R_1 + R_2)$$

$$I_2 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_B = I_2 * R_2$$

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$V_B = V_{BE} + V_E$$

$$V_E = V_B - V_{BE}$$

The emitter current I_E is given by;

$$I_E = \frac{V_E}{R_E}$$

$$\text{And } I_C \approx I_E$$

From KVL equation of collector-emitter circuit we get;

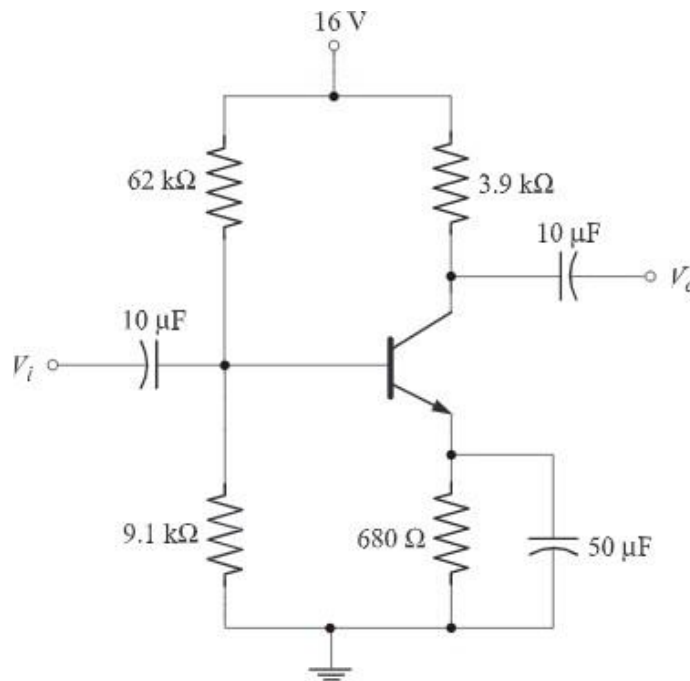
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Solved Examples:

Example 1:

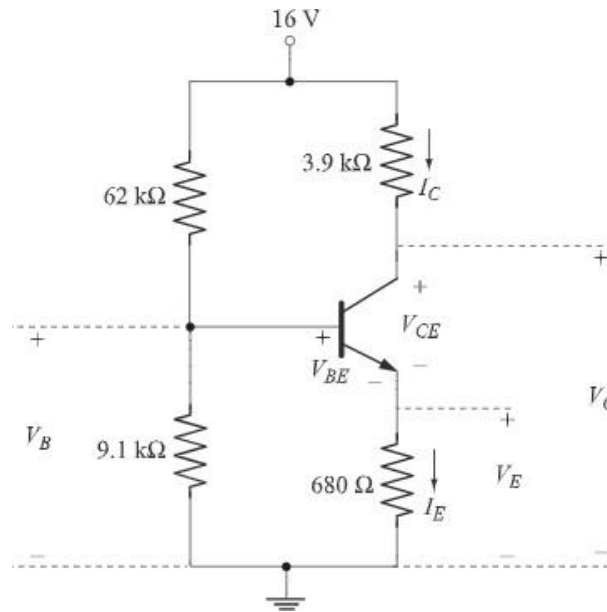
- Find the quiescent base current, collector current and V_{CE} for the circuit shown using silicon transistor with $V_{BE} = 0.7V$ and $\beta = 80$.
- Determine the values of collector, emitter and base voltages with respect to ground.
- Repeat (a) for $\beta = 150$.
- Draw the dc load line and locate the Q-points corresponding to two ' β ' values.



Solution:

Given Data: $V_{CC} = 16V$, $R_1 = 62k\Omega$, $R_2 = 9.1k\Omega$, $R_C = 3.9k\Omega$, $R_E = 680\Omega$, $C_1 = C_2 = 10\mu F$, $C_E = 50\mu F$, $V_{BE} = 0.7V$ and $\beta = 80$.

The dc equivalent circuit is shown below.



a. Base current, Collector current and Collector-Emitter Voltage.

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{62k \cdot 9.1k}{62k + 9.1k} = 7.94k\Omega$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{16 \cdot 9.1k}{62k + 9.1k} = 2.05V$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E} = \frac{2.05 - 0.7}{7.94k + (1 + 80)680} = 21.42\mu A$$

$$I_C = \beta I_B = 80 \cdot 21.42 \mu = 1.71 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 16 - 1.71m (3.9k + 680) = 8.17V$$

b. Collector, emitter and base voltages with respect to ground.

$$V_C = V_{CC} - I_C R_C = 16 - (1.71m \cdot 3.9k) = 9.33 \text{ V}$$

$$V_E = I_E R_E \approx I_C R_C = (1.71m \cdot 3.9k) = 1.16 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 + 1.16 = 1.86V$$

c. For $\beta = 150$: Base current, Collector current and Collector-Emitter Voltage.

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E} = \frac{2.05 - 0.7}{7.94k + (1 + 150)680} = 12.2\mu A$$

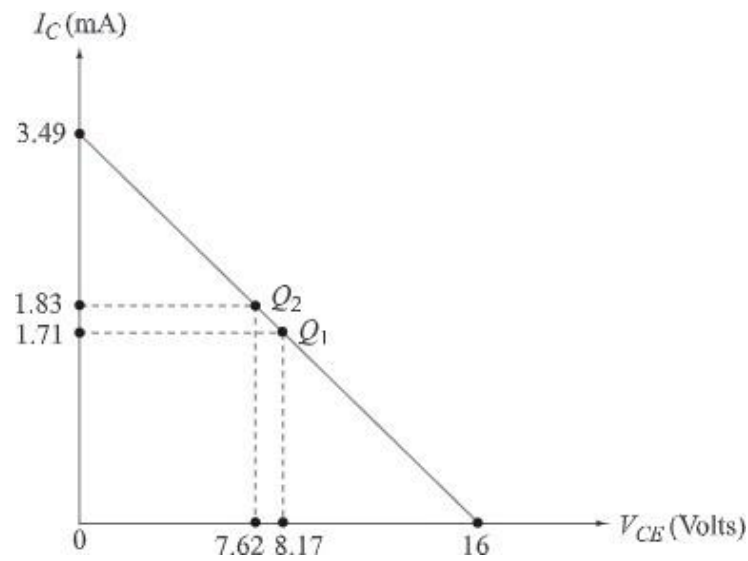
$$I_C = \beta I_B = 150 \cdot 12.2 \mu = 1.83 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 16 - 1.83m (3.9k + 680) = 7.62V$$

d. DC load line curve:

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{16}{3.9k + 680} = 3.49mA$$

β	I_{BQ}	I_{CQ}	V_{CEQ}
80	21.42 μA	1.71 mA	8.17 V
150	12.2 μA	1.83 mA	7.62 V



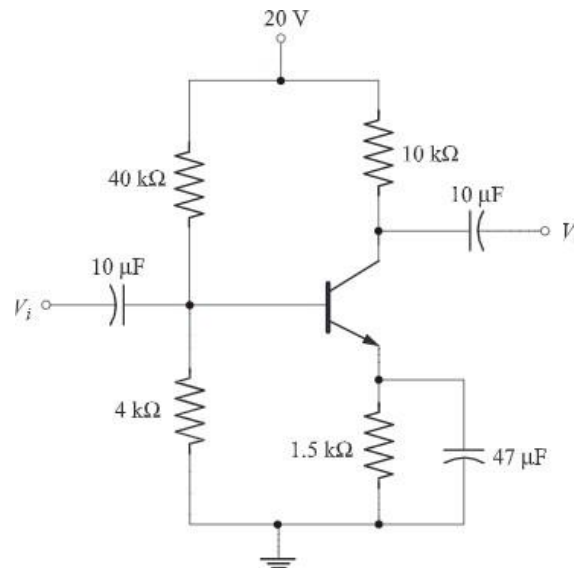
DC load line curve

Example 2:

For the voltage divider bias configuration shown below, Find

- IC and VCE using exact analysis
- IC and VCE using approximate analysis
- IC(sat)
- Compare the results obtained in (a) and (b) and comment

Assume silicon transistor with $\beta = 150$.


Solution:

Given Data: $V_{CC} = 20V$, $R_1 = 40k\Omega$, $R_2 = 4k\Omega$, $R_C = 10k\Omega$, $R_E = 1.5k\Omega$, $C_1 = C_2 = 10\mu F$, $C_E = 47\mu F$, $V_{BE} = 0.7V$ and $\beta = 150$.

a. Exact Analysis:

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{40k * 4k}{40k + 4k} = 3.63k\Omega$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{20 * 4k}{40k + 4k} = 1.82V$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E} = \frac{1.82 - 0.7}{3.63k + (1 + 150)1.5k} = 4.86\mu A$$

$$I_C = \beta I_B = 150 * 4.86 \mu = \mathbf{0.729 \text{ mA}}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 0.729m (10k + 1.5k) = \mathbf{11.62V}$$

b. Approximate Analysis:

$$\beta R_E = 150 \times 1.5k = 225k\Omega$$

$$10R_2 = 10 \times 4k = 40k\Omega$$

Note that $\beta R_E > 10R_2$, hence we can use approximate analysis.

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = 1.82 \text{ V (Same as } V_{Th} \text{)}$$

$$V_E = V_B - V_{BE} = 1.82 - 0.7 = 1.12 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.12}{1.5k} = 0.746 \text{ mA}$$

$$I_C \approx I_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 0.746m (10k + 1.5k) = 11.42V$$

c.

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{20}{10k + 1.5k} = 1.74mA$$

d. The results of exact and approximate analysis are compared in the following table.

<i>Parameter</i>	<i>Exact analysis</i>	<i>Approximate analysis</i>
I_C	0.729 mA	0.746 mA
V_{CE}	11.62 V	11.42 V

Transistor Switching Networks and Switching Characteristics

To operate BJT as a switch, it is to be operated in two regions namely, **cut-off and saturation region**. In cut-off region both the junctions are reverse biased and only reverse current flows which is very small and can be neglected. Thus no current flows through transistor in cut-off region, hence it acts as **open switch**. (Figure 9)

In saturation region both the junctions are forward biased. The voltage V_{CE} drops to very small value about **0.2V to 0.3V**. The collector current is very large and controlled by external resistance in collector circuit. Thus the transistor acts as a **closed switch**. (Figure 10)

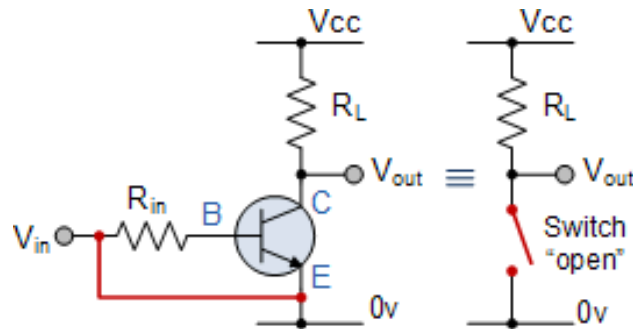


Fig.9: Cut-off region (Open switch)

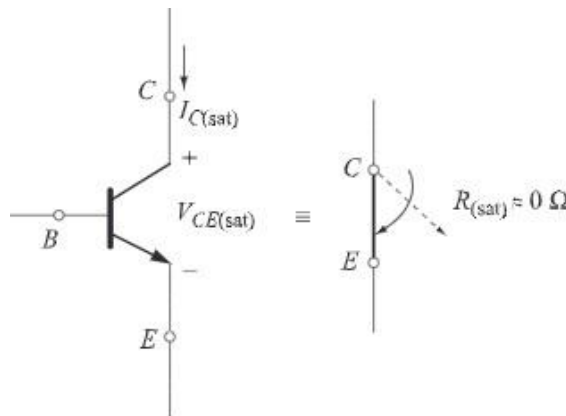


Fig.10: Saturation region (Closed switch)

Switching Characteristics:

When the base current is applied, the transistor does not switch on immediately. This is because of **junction capacitance and the transition time of electrons** across the junctions. The time between the application of input pulse and the commencement of current flow is termed as **delay time, T_d** . The time required for the collector current to reach **90% of its maximum level** from 10% level is called **rise time, T_r** . The turn-on time is the addition of rise time and delay time ($T_{on} = T_d + T_r$).

When the input current is switched off, the collector current does not go to zero level immediately. It goes to zero level after turn-off time, **which is the sum of storage time T_s , and**

fall time T_f . The fall time is specified as the time required for collector current to go from 90% to 10% of its maximum level. **The switching characteristic of transistor is shown in figure 1.28.**

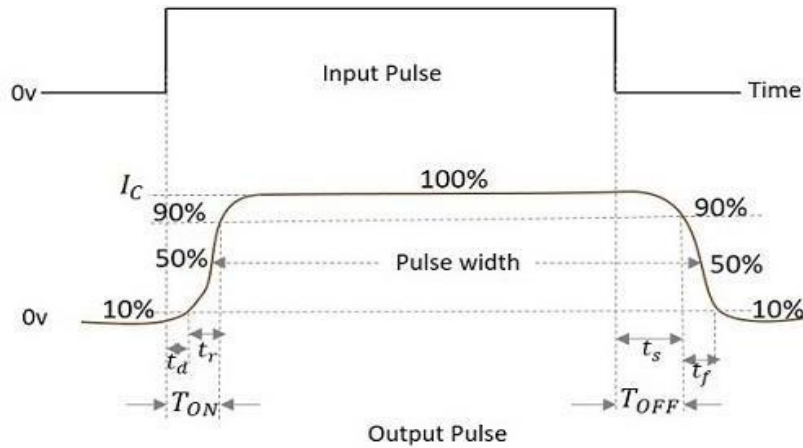


Fig.11: Transistor switching characteristics

Stability factors

The operating point of the transistor is affected by the parameters **reverse leakage current I_{CO} , current gain β and Base-emitter voltage drop V_{BE}** with variation in temperature. The transistor biasing circuits are to provide stability of collector current against the variations in I_{CO} , β and V_{BE} . The stability factor indicates the **degree of change in operating point due to variation in temperature.**

$$\left(\frac{\partial I_{CO}}{\partial I_{CO}} \right) = - \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } V_{BE} \text{ are constant}$$

$$\left(\frac{\partial V_{BE}}{\partial V_{BE}} \right) = - \frac{\Delta I_C}{\Delta V_{BE}}, \beta \text{ and } I_{CO} \text{ are constant}$$

$$(\beta) = \frac{\partial I_C}{\partial \beta} = \frac{\Delta}{\Delta \beta}, V_{BE} \text{ and } I_{CO} \text{ are constant}$$

$$I_C = I_{CEO} + \beta I_B$$

$$I_C = (1+\beta)I_{CBO} + \beta I_B$$

When I_{CBO} changes by ∂I_{CBO} , I_B changes by ∂I_B and I_C changes by ∂I_C we get;

$$\partial I_C = (1+\beta) \partial I_{CBO} + \beta \partial I_B$$

$$1 = (1+\beta) \frac{\partial I_C}{\partial I_C} + \beta \frac{\partial I_B}{\partial I_C}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_C}{\partial I_C}$$

$$\frac{\partial I_{CBO}}{\partial I_C} = [1 - \beta \frac{\partial I_B}{\partial I_C}] / (1 + \beta)$$

Frequency curve of an RC coupled amplifier

A practical amplifier circuit is meant to raise the voltage level of the input signal. This signal may be obtained from anywhere e.g. radio or TV receiver circuit. Such a signal is not of a single frequency. But it consists of a band of frequencies, e.g. from 20 Hz to 20 KHz. If the loudspeakers are to reproduce the sound faithfully, the amplifier used must amplify all the frequency components of signal by same amount. If it does not do so, the output of the loudspeaker will not be the exact replica of the original sound. When this happens then it means distortion has been introduced by the amplifier. Consider an RC coupled amplifier circuit shown in fig.1.

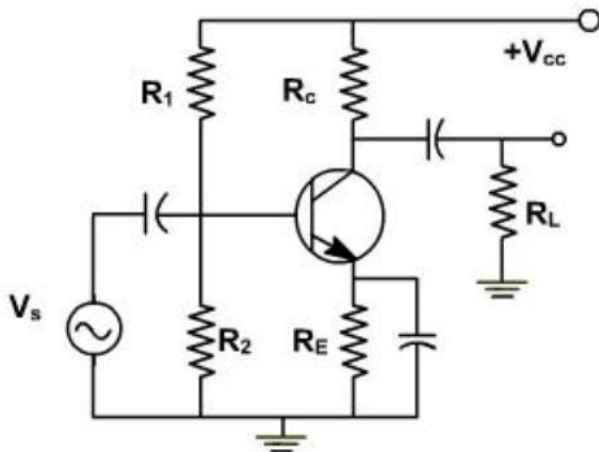


Fig:1

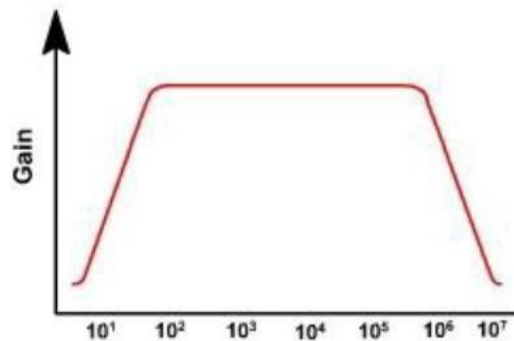


Fig: 2

Fig. 2 shows frequency response curve of a RC coupled amplifier. The curve is usually plotted on a semi-log graph paper with frequency range on logarithmic scale so that large frequency range can be accommodated. The gain is constant for a limited band of frequencies. This range is called mid-frequency band and gain is called mid band gain. AVM. On both sides of the mid frequency range, the gain decreases. For very low and very high frequencies the gain is almost zero. In mid band frequency range, the coupling capacitors and bypass capacitors are as good as short circuits. But when the frequency is low, these capacitors can no longer be replaced by the short circuit approximation.

$$X_C = \frac{1}{2\pi f C}$$

i.e. $X_C \propto \frac{1}{f}$

First consider coupling capacitor. The ac equivalent is shown in **fig. 3**, assuming capacitors are offering some impedance. In mid-frequency band, the capacitors are ac shorted so the input voltage

appears directly across r'_e but at low frequency the X_C is significant and some voltage drops across X_C . The input V_{in} at the base decreases and thus decreasing output voltage. The lower the frequency the more will be X_C and lesser will be the output voltage.

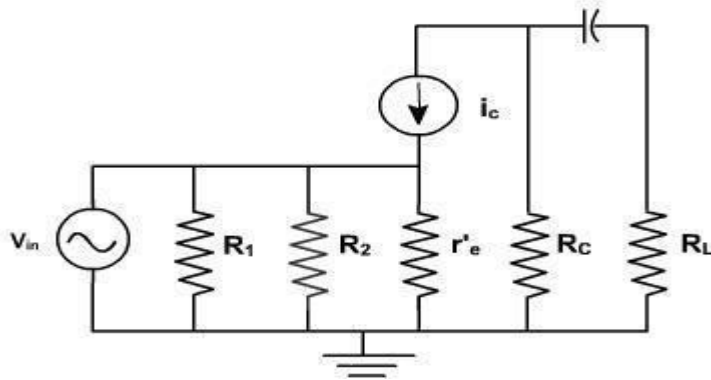


Fig 3

Similarly at low frequency, output capacitor reactance also increases. The voltage across R_L also reduces because some voltage drop takes place across X_C . Thus output voltage reduces. The X_C reactance not only reduces the gain but also change the phase between input and output. It would not be exactly 180° but decided by the reactance. At zero frequency, the capacitors are open circuited therefore output voltage reduces to zero.

The other component due to which gain decreases at low frequencies is the bypass capacitor. The function of this capacitor is to bypass ac and blocks dc. The impedance of this capacitor in mid frequency band is very low as compared to R_E so it behaves like ac short but as the frequency decrease the X_{CE} becomes more and no longer behaves like ac short. Now the emitter is not ac grounded. The ac emitter current i.e. divides into two parts i_1 and i_2 , as shown in **fig. 4**. A current i_1 passes through R_E and rest of the current passes through C . Due to ac current i_1 in R_E , an ac voltage is developed $i_1 * R_E$. With the polarity marked at an instant. Thus the effective V_L voltage is given by $V_{be} = V_s * R_E$.

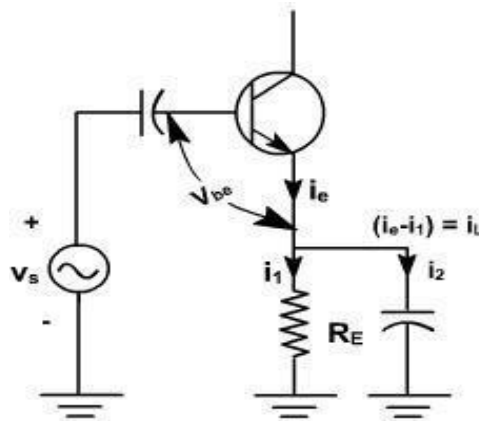


Fig 4

Thus the effective voltage input is reduced. The output also reduces. The lower the frequency, the lesser will be the gain. This reduction in gain is due to negative feedback.

As the frequency of the input signal increases, again the gain of the amplifier reduces. Firstly the gain of the transistor decreases at higher frequency and thus reducing the voltage gain of the amplifier at higher frequencies as shown in **fig.5**.

The other factor responsible for the reduction in gain at higher frequencies is the presence of various capacitors as shown in **fig. 6**. They are not physically connected but inherently present with the device.

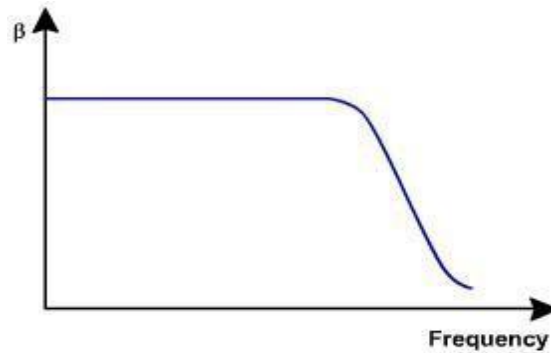


Fig 5

The capacitor C_{bc} between the base and the collector connects the output with the input. Because of this, negative feedback takes place in the circuit and the gain decreases. This feedback effect is more, when C_{bc} provides a path for higher frequency ac currents. The capacitance C_{be} offers a low input impedance at higher frequency thus reduces the effective input signal and so the gain falls. Similarly, C_{ce} provides a shunting effect at high frequencies in the output side and reduces gain of the amplifier.

Besides these junction capacitances there are wiring capacitance C_{w1} and C_{w2} . The reactance is very small but at high frequencies they become 5 to 20p.f. For a multistage amplifier, the effect of the capacitances C_{ce} , C_{w1} and C_{w2} can be represented by single shunt capacitance. $C_S = C_{w1} + C_{w2} + C_{ce}$. At higher frequency, the capacitor C_S offers low input impedance and thus reduces the output.

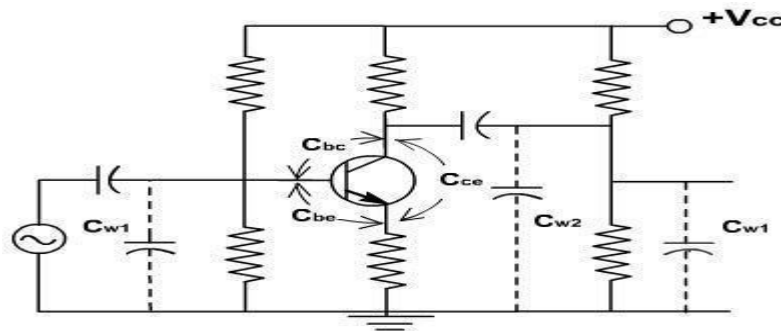


Fig 6

Bandwidth of an amplifier:

The gain is constant over a frequency range. The frequencies at which the gain reduces to 70.7% of the maximum gain are known as cut off frequencies, upper cut off and lower cut off frequency. **fig.7**, shows these two frequencies. The difference of these two frequencies is called Band width (BW) of an amplifier. $BW = f_2 * f_1$.

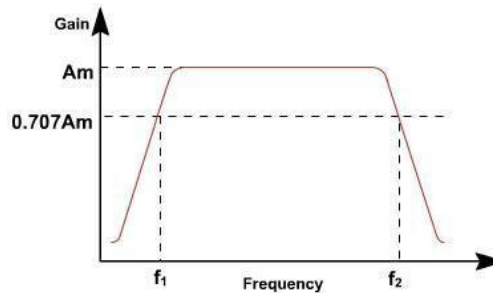


Fig 7

At f_1 and f_2 , the voltage gain becomes $0.707 A_m$. The output voltage reduces to $\frac{1}{\sqrt{2}}$ of maximum output voltage. Since the power is proportional to voltage square, the output power at these frequencies becomes half of maximum power. The gain on dB scale is given by $20 \log_{10} (V_2 / V_1) = 20 \log_{10} (0.707) = 10 \log_{10} (1 / \sqrt{2})^2 = 10 \log_{10} (1 / 2) = -3 \text{ dB}$. If the difference in gain is more than 3 dB, then it can be detected by human. If it is less than 3 dB it cannot be detected.

Direct Coupling:

For applications, where the signal frequency is below 10 Hz, coupling and bypass capacitors cannot be used. At low frequencies, these capacitors can no longer be treated as ac short circuits, since they offer very high impedance. If these capacitors are used then their values have to be extremely large e.g. to bypass a 100 ohm emitter resistor at 10 Hz, we need a capacitor of approximately 1600micro Farad. The lower the frequency the worse the problem becomes.

To avoid this, direct coupling is used. This means designing the stages without coupling and bypass capacitors, so that the direct current is coupled as well as alternating current. As a result, there is no lower frequency limit. The amplifier enlarges the signal no matter have low frequency including dc or zero frequency.

h-Parameters

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

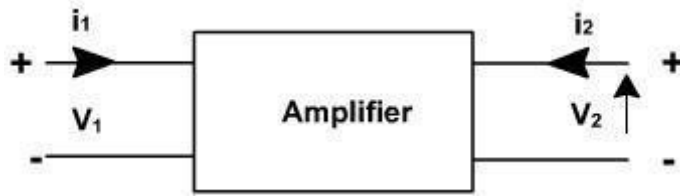


Fig 1

Out of four quantities two are independent and two are dependent. If the input current i_1 and output voltage V_2 are taken independent, then other two quantities i_2 and V_1 can be expressed in terms of i_1 and V_2 .

$$V_1 = f_1(i_1, V_2)$$

$$i_2 = f_2(i_1, V_2)$$

The equations can be written as

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$i_2 = h_{21} i_1 + h_{22} V_2$$

Where h_{11} , h_{12} , h_{21} and h_{22} are called h-parameters.

$$h_{11} = \left. \frac{V_1}{i_1} \right|_{V_2 = 0}$$

h_{11} = input impedance with output short circuit to ac.

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{i_2 = 0}$$

h_{12} = fraction of output voltage at input with input open circuited or reverse voltage gain with input open circuited to ac

$$h_{21} = \left. \frac{i_2}{i_1} \right|_{V_2 = 0}$$

h_{21} = negative of current gain with output short circuited to ac. The current entering the load is negative of i_2 . This is also known as forward short circuit current gain.

$$h_{22} = \left. \frac{i_2}{V_2} \right|_{i_1 = 0}$$

h_0 = output admittance with input open circuited to ac. If these parameters are specified for a particular configuration, then suffixes e, b or c are also included, e.g. h_{fe} , h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in **fig. 2**.

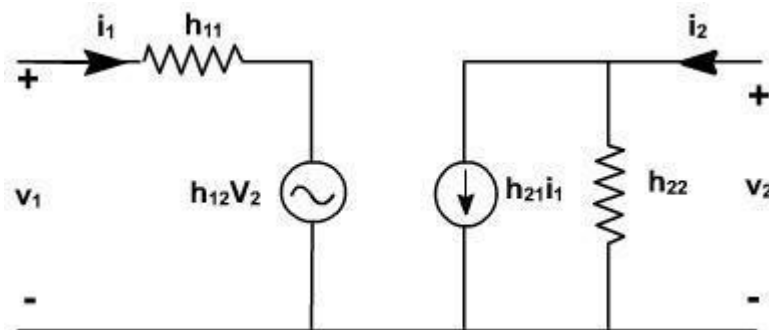


Fig 2

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in **fig. 3**. The variables, i_B , i_C , v_C , and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B , I_C as dependent variables.

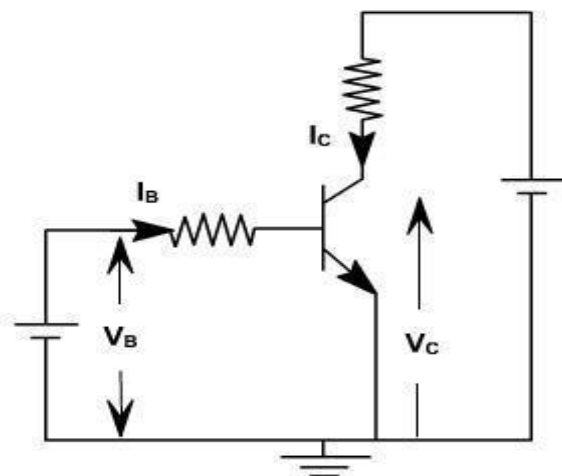


Fig 3

$$V_B = f_1(i_B, V_C) \quad I_C = f_2(i_B, V_C).$$

Using Taylor's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left. \frac{\partial f_1}{\partial i_B} \right|_{v_C} \Delta i_B + \left. \frac{\partial f_1}{\partial v_C} \right|_{i_B} \Delta v_C$$

$$\Delta i_C = \left. \frac{\partial f_2}{\partial i_B} \right|_{v_C} \Delta i_B + \left. \frac{\partial f_2}{\partial v_C} \right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B , Δv_C , Δi_B , Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as V_b , I_b , V_C , I_C

$$\therefore v_b = h_{ie} i_b + h_{re} v_C$$

$$i_C = h_{fe} i_b + h_{oe} v_C$$

where

$$h_{ie} = \left. \frac{\partial f_1}{\partial i_B} \right|_{v_C} = \left. \frac{\partial v_B}{\partial i_B} \right|_{v_C}; \quad h_{re} = \left. \frac{\partial f_1}{\partial v_C} \right|_{i_B} = \left. \frac{\partial v_B}{\partial v_C} \right|_{i_B}$$

$$h_{fe} = \left. \frac{\partial f_2}{\partial i_B} \right|_{v_C} = \left. \frac{\partial i_C}{\partial i_B} \right|_{v_C}; \quad h_{oe} = \left. \frac{\partial f_2}{\partial v_C} \right|_{i_B} = \left. \frac{\partial i_C}{\partial v_C} \right|_{i_B}$$

The model for CE configuration is shown in **fig. 4**.

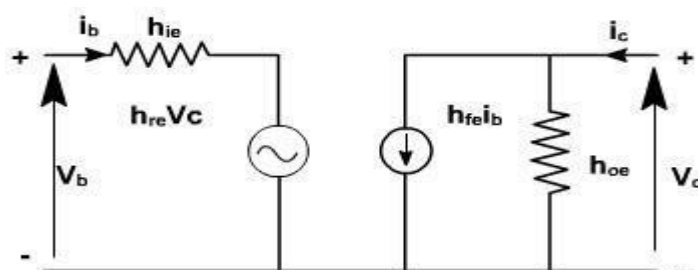


Fig 4

Determination of h - parameters:

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. **Fig.5**, shows the output characteristics of CE amplifier.

$$h_{fe} = \left. \frac{\partial i_C}{\partial i_B} \right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}}$$

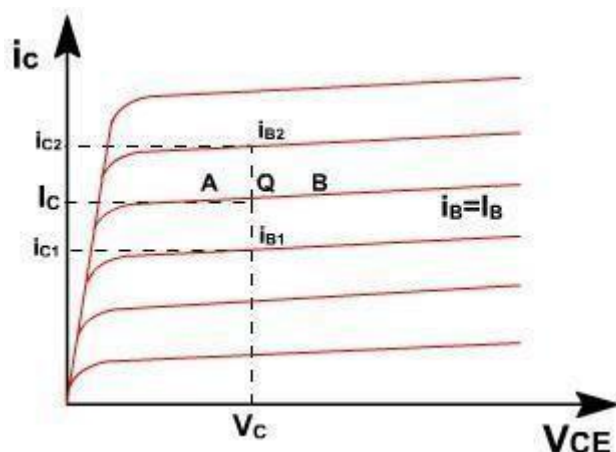


Fig 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left. \frac{\partial i_c}{\partial V_C} \right|_{i_B}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left. \frac{\Delta V_B}{\Delta i_B} \right|_{V_C}$$

h_{ie} is the slope of the appropriate input on **fig. 6**, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left. \frac{\Delta V_B}{\Delta V_C} \right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

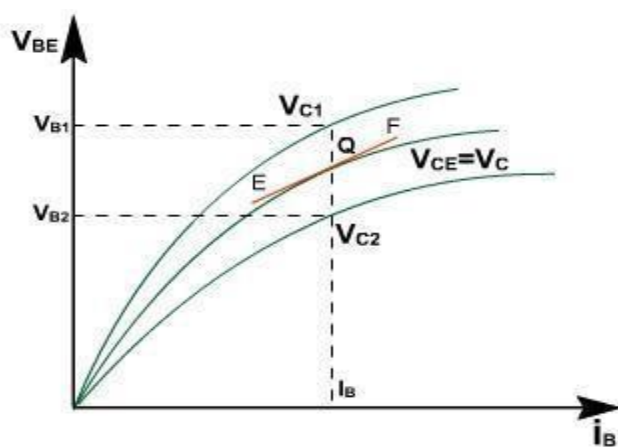


Fig6

A vertical line on the input characteristic represents constant base current. The parameter h_{re} can be obtained from the ratio $(V_{B2}: V_{B1})$ and $(V_{C2}: V_{C1})$ for at Q.

Analysis of a transistor amplifier using h-parameters:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in **fig. 1** and to bias the transistor properly.

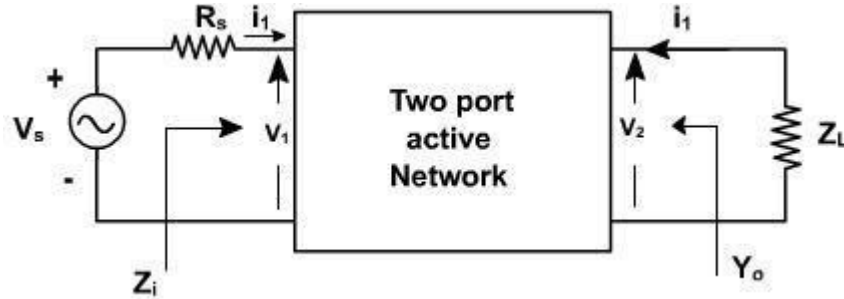


Fig 1

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedance h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in **fig. 2**. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedance, voltage gain, and output impedance.

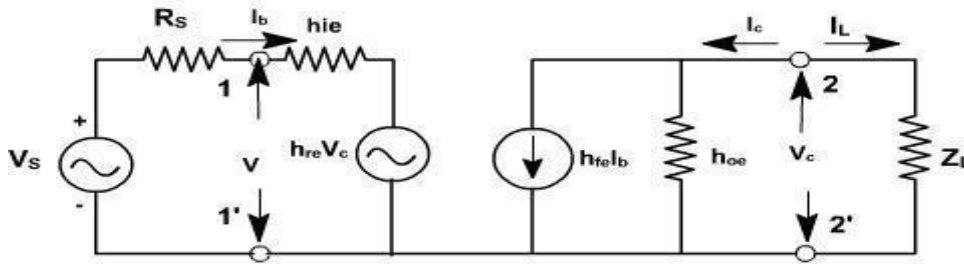


Fig 2

Current gain: For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{i_L}{i_b} = \frac{-i_c}{i_b} \quad (i_L + i_c = 0 \quad \therefore i_L = -i_c)$$

$$i_c = h_{fe} i_b + h_{oe} V_c$$

$$V_c = i_L Z_L = -i_c Z_L$$

$$\therefore i_c = h_{fe} i_b + h_{oe} (-i_c Z_L)$$

$$\text{or } \frac{i_c}{i_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_i = - \frac{h_{fe}}{1 + h_{oe} Z_L}$$

Input Impedance: The impedance looking into the amplifier input terminals (1, 1') is the input impedance Z_i .

$$\begin{aligned}
 Z_i &= \frac{V_b}{I_b} \\
 V_b &= h_{ie} I_b + h_{re} V_c \\
 \frac{V_b}{I_b} &= h_{ie} + h_{re} \frac{V_c}{I_b} \\
 &= h_{ie} - \frac{h_{re} I_c Z_L}{I_b} \\
 \therefore Z_i &= h_{ie} + h_{re} A_i Z_L \\
 &= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L} \\
 \therefore Z_i &= h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \quad (\text{since } Y_L = \frac{1}{Z_L})
 \end{aligned}$$

Voltage gain: The ratio of output voltage to input voltage gives the gain of the transistors.

$$\begin{aligned}
 A_v &= \frac{V_c}{V_b} = - \frac{I_c Z_L}{V_b} \\
 \therefore A_v &= \frac{I_b A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}
 \end{aligned}$$

Output Admittance: It is defined as

$$\begin{aligned}
 Y_o &= \left. \frac{I_c}{V_c} \right|_{V_s=0} = 0 \\
 I_c &= h_{fe} I_b + h_{oe} V_c \\
 \frac{I_c}{V_c} &= h_{fe} \frac{I_b}{V_c} + h_{oe} \\
 \text{when } V_s &= 0, \quad R_s I_b + h_{ie} I_b + h_{re} V_c = 0. \\
 \frac{I_b}{V_c} &= - \frac{h_{re}}{R_s + h_{ie}} \\
 \therefore Y_o &= h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}
 \end{aligned}$$

Voltage amplification taking into account source impedance (R_s) is given by

$$\begin{aligned}
 A_{vs} &= \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_s} \quad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i \right) \\
 &= A_v * \frac{Z_i}{Z_i + R_s} \\
 &= \frac{A_i Z_L}{Z_i + R_s}
 \end{aligned}$$

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_S in parallel with a resistance R_S as shown in **fig. 3**.

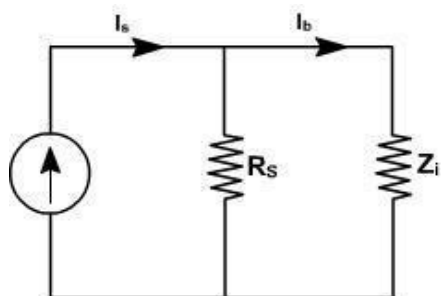


Fig 3

In this case, overall current gain AIS is defined as

$$\begin{aligned}
 A_{I_s} &= \frac{I_L}{I_s} \\
 &= -\frac{I_c}{I_s} \\
 &= -\frac{I_c}{I_b} \cdot \frac{I_b}{I_s} \quad \left(I_b = \frac{I_s \cdot R_s}{R_s + Z_i} \right) \\
 &= A_I \cdot \frac{R_s}{R_s + Z_i}
 \end{aligned}$$

To analyze multistage amplifier, the parameters of the transistor used are obtained from manufacture data sheet. The h -parameters usually provides h -parameter in CE configuration. These parameters may be converted into CC and CB values. For example h_{rc} in terms of CE parameter can be obtained as follows.

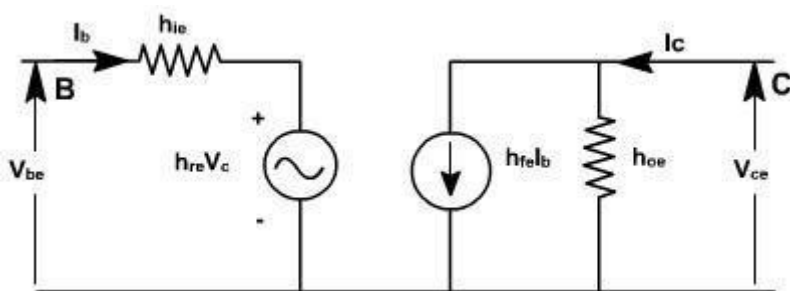


Fig 4

For CE transistor configuration $V_{be} = h_{ie} I_b + h_{re} V_{ce}$ $I_c = h_{fe} I_b + h_{oe} V_{ce}$
 The circuit can be redrawn like CC transistor configuration as shown in **fig. 5**.
 $V_{bc} = h_{ie} I_b + h_{rc} V_{ec}$ $I_c = h_{fe} I_b + h_{oe} V_{ec}$

$$\begin{aligned}
 h_{rc} &= \left. \frac{V_{be}}{V_{ec}} \right|_{I_b=0} \\
 &= \left. \frac{V_{be} + V_{ec}}{V_{ec}} \right|_{I_b=0} \\
 &= \left. \left(\frac{V_{be}}{V_{ec}} + 1 \right) \right|_{I_b=0}
 \end{aligned}$$

Since $I_b = 0$, $V_{be} = h_{re} V_c = -h_{re} V_{ec}$

$$\begin{aligned}
 \therefore h_{rc} &= 1 + \left(\frac{h_{re} V_{ec}}{V_{ec}} \right) \\
 &= 1 - h_{re}
 \end{aligned}$$

Similarly

$$\begin{aligned}
 h_{fc} &= \left. \frac{I_e}{I_b} \right|_{V_{ec}=0} = \left. \frac{-(I_b + I_c)}{I_b} \right|_{V_{ec}=0} \\
 &= -(1 + h_{fe})
 \end{aligned}$$

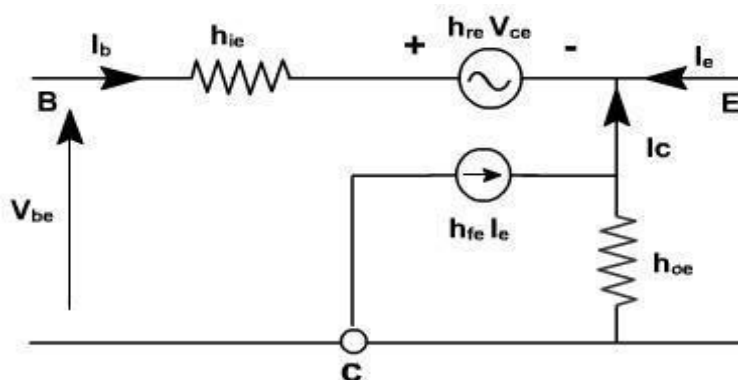


Fig 5

Simplified common emitter hybrid model:

In most practical cases it is appropriate to obtain approximate values of A_V , A_i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig. 6** shows the CE amplifier equivalent circuit in terms of h-parameters. Since $1/h_{oe}$ in parallel with R_L is approximately equal to R_L if $1/h_{oe} \gg R_L$ then h_{oe} may be neglected. Under these conditions,

$$I_c = h_{fe} I_b$$

$$h_{revc} = h_{re} I_c R_L = h_{re} h_{fe} I_b R_L$$

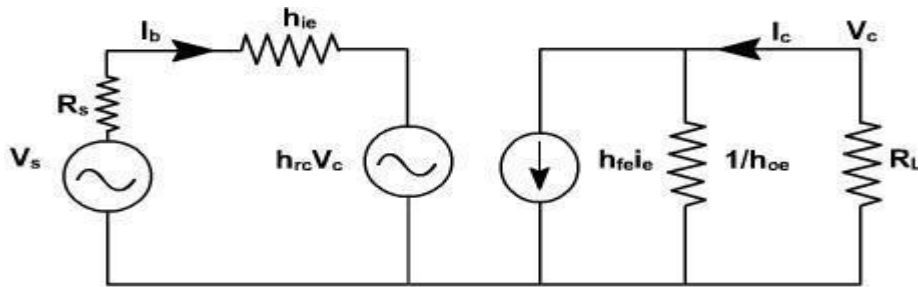


Fig 6

Since h_{fe} , $h_{re} = 0.01$, this voltage may be neglected in comparison with i_c , I_b drop across h_{ie} provided R_L is small than h_{oe} and hence h_{re} can be neglected.

$$A_i = -\frac{h_{fe}}{1 + h_{oe} R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_v = \frac{A_i R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedance seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we find $I_b = 0$, $I_c = 0$. True value depends upon R_S and lies between 40 K and 80K. On the same lines, the calculations for CC and CB [can be done](#).

CE amplifier with an emitter resistor:

The voltage gain of a CE stage depends upon h_{fe} . This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_v of each stage, it should be independent of h_{fe} . A simple and effective way is to connect an emitter resistor R_e as shown in **fig. 7**. The resistor provides negative feedback and stabilization.

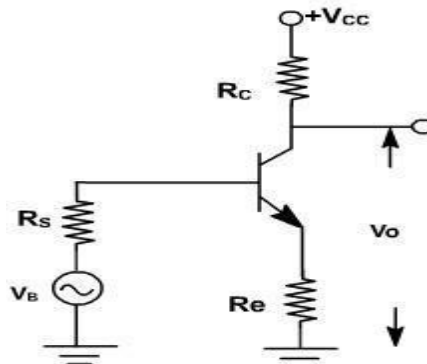


Fig 7

An approximate analysis of the circuit can be made using the simplified model.

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe} I_b}{I_b} \\ = -h_{fe}$$

It is unaffected by the addition of R_C .

Input resistance is given by

$$R_i = \frac{V_i}{I_b} \\ = \frac{h_{ie} I_b + (1+h_{fe}) I_b R_e}{I_b} \\ = h_{ie} + (1+h_{fe}) R_e$$

The input resistance increases by $(1+h_{fe}) R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe} R_L}{h_{ie} + (1+h_{fe}) R_e}$$

Clearly, the addition of R_e reduces the voltage gain.

If $(1+h_{fe}) R_e \gg h_{ie}$ and $h_{fe} \gg 1$

then

$$A_v = \frac{-h_{fe} R_L}{(1+h_{fe}) R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation A_v is completely stable. The output resistance is infinite for the approximate model.